Jitter Analysis

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Phase fluctuation is a main cause of errors on networks based on E1 such as private lines, ISDN, FRL. That is the reasons why it is so important to keep Jitter under control when managing E1 nodes and Circuits. Additionally E1 signal is very suitable for synchronization and it is a good to keep it in a good shape.

This operation can be done using the new Aurora Tango E1 which performs Jitter measurements such as level, tolerance and transfer.

Aurora Tango E1

International Marketing Dpt.

Network Synchronization

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Jitter and Network Synchronization

Synchronization is the set of techniques that enable the frequency and phase of the equipment clocks in a network to remain constrained within the specified limits (see Figure 0.1). The first digital networks were asynchronous, and therefore did not call for properly working external synchronization. It was the arrival of SDH and SONET networks that started to make synchronization essential to maintain transmission quality and efficiency of supported teleservices.

Bad synchronization causes regeneration errors and *slips*. The effects of these impairments vary in different systems and services. Some isochronous[1] services, like telephony, tolerate a deficient synchronization rather well, and small or no effects can be observed by the end-user. Others, like digital TV transmission, fax, or compressed voice and video services, are more sensitive to synchronization problems. In HDLC, FRL, or TCP/IP types of data services, slips that occur force us to retransmit packets, and this makes transmission less efficient.

1.1 ARCHITECTURE OF SYNCHRONIZATION NETWORKS

Synchronization networks can have hierarchical or nonhierarchical architectures. Networks that use *hierarchical synchronization* have a tree architecture. In such networks a master clock is distributed, making the rest of the clocks slaves of its signal. A network with all the equipment clocks locked to a single master timing reference is called *synchronous*. The following elements can be found in the hierarchical synchronization network:

1. A *master clock*, which is usually an atomic cesium oscillator with global positioning system (GPS) and/or Loran-C[2] reference. It occupies the top of the pyramid, from which many synchronization levels spread out (see Table 1.1).

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[1] Isochronous (from the Greek "equal" and "time") pertains to processes that require timing coordination to be successful, such as voice and digital video transmission.

[2] Loran-C is an electronic position fixing system using pulsed signals at 100 kHz.

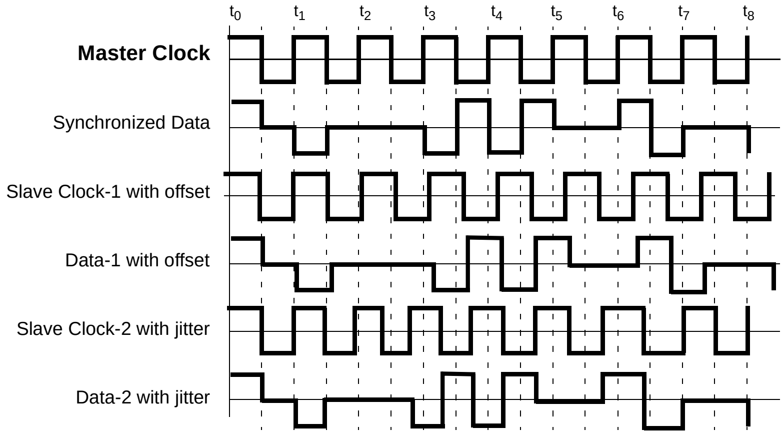


Figure 0.1 A master clock that marks the significant instances for data transmission. Clocks 1 and 2 are badly synchronized, and the data transmitted with these references is also affected by the same phase error.

2. High-quality *slave clocks*, to receive the master clock signal and, once it is filtered and regenerated, distribute it to all the NEs of their node.
3. *NE clocks*, which finish the branches of the tree by taking up the lowest levels of the synchronization chain. Basically, they are the ones using the clock, although they may also send it to other NEs.
4. *Links*, responsible for transporting the clock signal. They may belong to the synchronization network only, or, alternatively, form a part of a transport network, in which case the clock signal is extracted from data flow (see Figure 1.3).

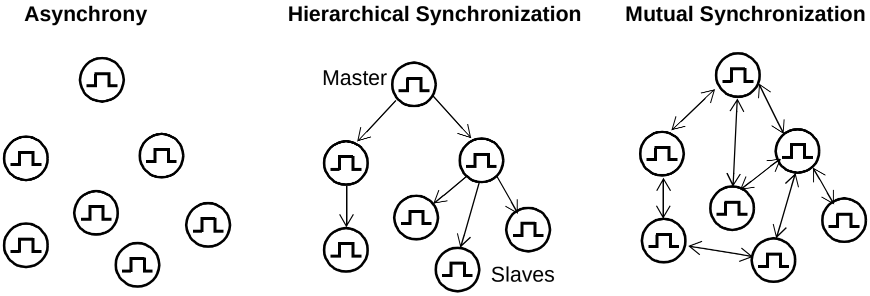


Figure 1.2 Classes of synchronization architectures.

The pure hierarchical synchronization architecture can be modified in several ways to improve network operation. *Mutual synchronization* is based on cooperation between nodes to choose the best possible clock. There can be several master clocks, or even a cooperative synchronization network, besides a synchronization protocol between nodes (see Figure 1.2). Bringing these networks into services is more complex, although the final outcome is very solid.

Those networks where different nodes can use a clock of their own, and correct operation of the whole depends on the quality of each individual clock, are called *asynchronous* (see Figure 1.2). Asynchronous operation can only be used if the quality of the node clocks is good enough, or if the transmission rate is reduced. The operation of a network (that may be asynchronous in the sense described above or not) is classified as *plesiochronous* if the equipment clocks are constrained within margins narrow enough to allow simple bit stuffing (see Figure 1.2).

General requirements for today's SONET and SDH networks are that any NE must have at least two reference clocks, of higher or similar quality than the clock itself. All the NEs must be able to generate their own synchronization signal in case they lose their external reference. If such is the case, it is said that the NE is in *holdover*.

A synchronization signal must be filtered and regenerated by all the nodes that receive it, since it degrades when it passes through the transmission path, as we will see later.

Table 1.1
Clock performance.

Type	*Performance*
Cesium	From 10^{-11} up to 10^{-13}
Hydrogen	From 10^{-11} up to 10^{-13}
GPS	Usually 10^{-12}
Rubidium	From 10^{-9} up to 10^{-10}
Crystal	From 10^{-5} up to 10^{-9}

1.1.1 Synchronization Network Topologies

The synchronization and transport networks are partially mixed, since some NEs both transmit data and distribute clock signals to other NEs.

The most common topologies are:

1. *Tree*: This is a basic topology that relies on a master clock whose reference is

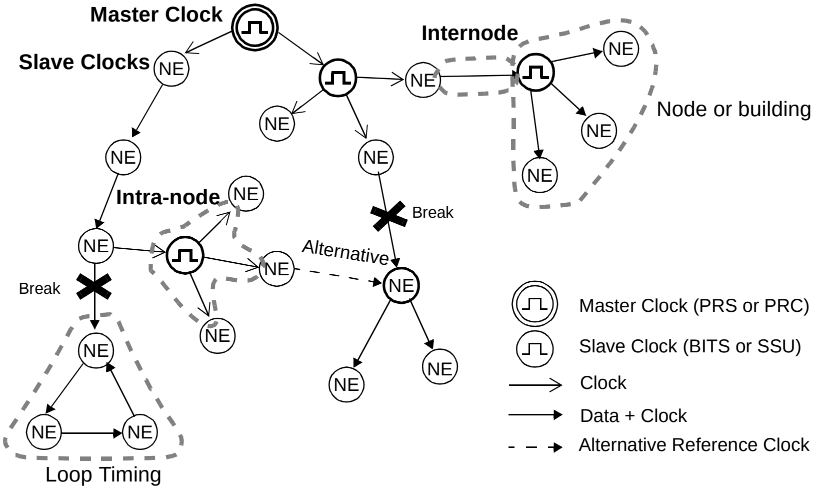


Figure 1.3 Synchronization network topology for SONET and SDH. This figure does not show links that are for transport only.

distributed to the rest of the slave clocks. It has two weak points: it depends on only one clock, and the signals gradually degrade (see Figure 1.5).

2. *Ring*: Basically, this is a tree topology that uses SDH/SONET ring configurations to propagate the synchronization signal. The ring topology offers a way to make a tree secure, but care must be taken to avoid the formation of synchronizing loops.
3. *Distributed*: Nodes make widespread use of many primary clocks. The complete synchronization network is formed by two or more islands; each of them depending on a different primary clock. To be rigorous, such a network is asynchronous, but thanks to the high accuracy of the clocks commonly used as a primary clock, the network operates in a very similar way to a completely synchronous network.
4. *Meshed*: In this topology, nodes form interconnections between each other, in order to have redundancy in case of failure. However, synchronization loops occur easily and should be avoided.

Synchronization networks do not usually have only one topology, but rather a combination of all of them. Duplication and security involving more than one master clock, and the existence of some kind of synchronization management protocol, are important features of modern networks. The aim is to minimize the problems associated with signal transport, and to avoid depending on only one clock in case of failure. As a result, we get an extremely precise, redundant, and solid synchronization network.

1.2 INTERCONNECTION OF NODES

There are two basic ways to distribute synchronization across the whole network:

- *Intranode,* which is a high-quality slave clock known as either *synchronization supply unit* (SSU) or *building integrated timing supply* (BITS). These are responsible for distributing synchronization to NEs situated inside the node (see Figure 1.3).
- *Internode,* where the synchronization signal is sent to another node by a link specifically dedicated to this purpose, or by an STM-*n*/OC-*m* signal (see Figure 1.3).

1.2.1 Synchronization Signals

There are several signals suitable for transporting synchronization:

- Analog, of 1,544 and 2,048 kHz;
- Digital, of 1,544 and 2,048 Kbps;
- STM-*n*/OC-*m* line codes, from which one of the above-mentioned signals is derived, by means of a specialized circuit.

In any case, it is extremely important for the clock signal to be continuous. In other words, its mean frequency should never be less than its fundamental frequency (see Figure 1.4).

1.2.1.1 Clock transfer across T-carrier/PDH networks

These types of networks are very suitable for transmitting synchronization signals, as the multiplexing and demultiplexing processes are bit oriented (not byte oriented like SONET and SDH), and justification is performed by removing or adding single bits. As a result, T1 and E1 signals are transmitted almost without being affected by

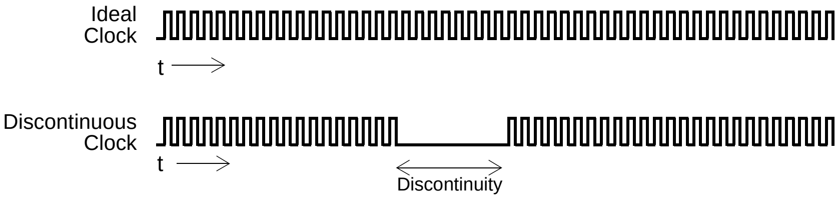


Figure 1.4 A pure clock signal is continuous, as, for example, the one provided by an atomic clock. A discontinuous signal in its turn could be a signal delivered by a T1 circuit transported in SONET.

justification jitter, mapping or overhead-originated discontinuities. This characteristic is known as *timing transparency.*

There is only one thing to be careful with, and that is to not let T1 and E1 signals cross any part of SONET or SDH, as they would be affected by phase fluctuation due to mapping processes, excessive overhead, and pointer movements. In short, T1 or E1 would no longer be suitable for synchronization.

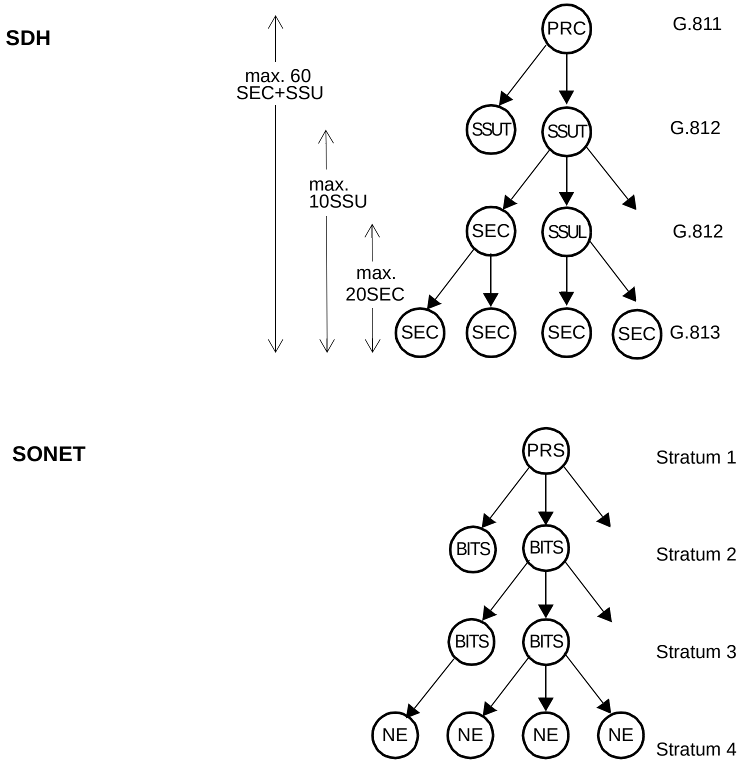
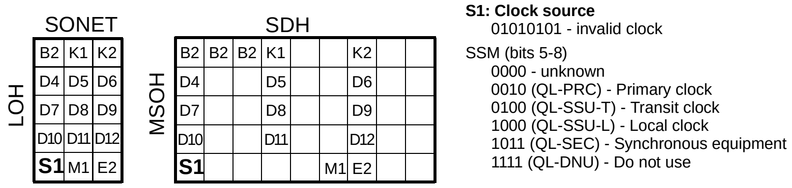


Figure 1.5 Synchronization network model for SONET and SDH. Stratum 3 has the minimum quality required for synchronizing an NE. In SDH the figures indicate the maximum number of clocks that can be chained together by one signal.

1.2.1.2 Clock transfer across SDH/SONET links

To transport a clock reference across SDH/SONET, a line signal is to be used instead of the tributaries transported, as explained before. The clock derived from an STM-*n*/OC-*m* interface is only affected by wander due to temperature and environmental reasons. However, care must be taken with the number of NEs to be chained together, as all the NEs regenerate the STM-*n*/OC-*m* signal with their own clock and, even if they were well synchronized, they would still cause small, accumulative phase errors.

The employment of STM-*n*/OC-*m* signals has the advantage of using the S1 byte to enable *synchronization status messages* (SSMs) to indicate the performance of the clock with which the signal was generated (see Figure 1.6). These messages are essential in reconstructing the synchronization network automatically in case of failure. They enable the clocks to choose the best possible reference, and, if none is available that offers the performance required, they enter the holdover state.



B2	K1	K2
D4	D5	D6
D7	D8	D9
D10	D11	D12
S1	M1	E2

B2	B2	B2	K1			K2		
D4			D5			D6		
D7			D8			D9		
D10			D11			D12		
S1					M1	E2		

S1: Clock source
01010101 - invalid clock
SSM (bits 5-8)
0000 - unknown
0010 (QL-PRC) - Primary clock
0100 (QL-SSU-T) - Transit clock
1000 (QL-SSU-L) - Local clock
1011 (QL-SEC) - Synchronous equipment
1111 (QL-DNU) - Do not use

Figure 1.6 The S1 byte is used to send SSMs in SDH and SONET.

1.2.2 Holdover Mode

It is said that a slave clock enters holdover mode when it decides to use its own generator, because it does not have any reference available, or the ones available do not offer the performance required. In this case, the equipment remembers the phase and the frequency of the previous valid reference, and reproduces it as well as possible. Under these circumstances, it puts an SSM=QL-SEC message into the S1 byte of STM-*n*/OC-*m* frames, and, if it was generating synchronization signals at 1.5 or 2 MHz, it stops doing so.

1.2.3 Global Positioning System

The *global positioning system* (GPS) is a constellation of 24 satellites that belongs to the U.S. Department of Defense. The GPS receivers can calculate, with extreme precision, their terrestrial position and the universal time from where they extract the synchronization signal. The GPS meets the performance required from a primary clock (see Table 1.1). However, the GPS system might get interfered with intentionally, and the U.S. Department of Defense reserves the right to deliberately degrade its performance for tactical reasons.

1.3 DISTURBANCES IN SYNCHRONIZATION SIGNALS

Since synchronization signals are distributed, degradation in the form of jitter and wander accumulate. At the same time they are affected by different phenomena that cause phase errors, frequency offset, or even the complete loss of the reference clock. Care must be taken to avoid degradation in the form of slips and bit errors by filtering and an adequate synchronization distribution architecture (see Figure 1.7).

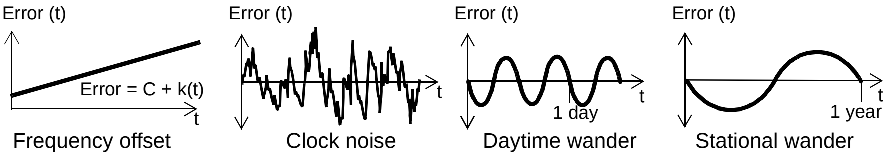


Figure 1.7 Sources of phase variation.

1.3.1 Frequency Offset

Frequency offset is an undesired effect that occurs during the interconnection of networks or services whose clocks are not synchronized. There are several situations where frequency deviations occur (see Figure 1.8):

- On the boundary between two synchronized networks with different primary reference clocks;
- When tributaries are inserted into a network by nonsynchronized ADMs;
- When, in a synchronization network, a slave clock becomes disconnected from its master clock and enters holdover mode.

1.3.2 Phase Fluctuation

In terms of time, the phase of a signal can be defined as the function that provides the position of any significant instant of this signal. It must be noticed that a time reference is necessary for any phase measurement, because only a phase relative to a reference clock can be defined. A significant instant is defined arbitrarily; it may for instance be a trailing edge or a leading edge, if the clock signal is a square wave (see Figure 1.9).

Here, when we talk about a phase, we think of it as being related to clock signals. Every digital signal has an associated clock signal to determine, on reception, the instants when to read the value of the bits that this signal is made up of. The clock recovery on reception circuits reads the bit values of a signal correctly when there is

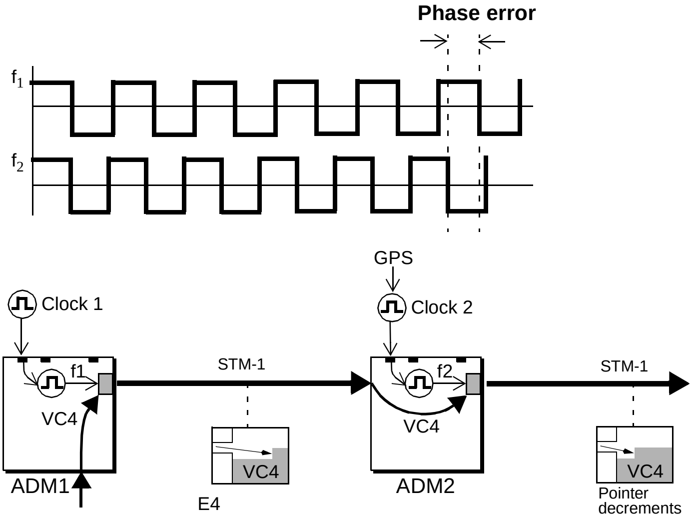


Figure 1.8 Comparison of two reference signals that synchronize two SDH multiplexers. Periodical pointer adjustment occurs due to the frequency offset there is between the two signals.

no phase fluctuation, or when there is very little. Nevertheless, when the clock recovery circuitry cannot track these fluctuations (absorb them), the sampling instants of the clock obtained from the signal may not coincide with the correct instants, producing bit errors.

When phase fluctuation is fast, this is called jitter. In the case of slow phase fluctuations, known as wander, the previously described effect does not occur.

Phase fluctuation has a number of causes. Some of these are due to imperfections in the physical elements that make up transmission networks, whereas others result from the design of the digital systems in these networks.

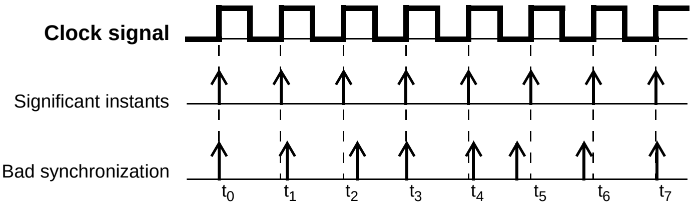


Figure 1.9 Phase error of a signal in relation to its ideal frequency.

1.3.2.1 Jitter

Jitter is defined as short-term variations of the significant instants of a digital signal from their reference positions in time, ITU-T Rec. G.810 (see Figure 1.10). In other words, it is a phase oscillation with a frequency higher than 10 Hz. Jitter causes sampling errors and provokes slips in the *phase-locked loops* (PLL) buffers (see Figure 1.11). There are a great many causes, including the following:

Jitter in regenerators

As they travel along line systems, SONET and SDH signals go through a radio-electrical, electrical, or optical process to regenerate the signals. But clock recovery in regenerators depends on the bit pattern transported by the signal, and the quality of the recovered clock becomes degraded if transitions in the pattern are distributed heterogeneously, or if the transition rate is too low. This effect can be countered by means of scrambling, which is used to destroy correlation of the user-generated bit sequence. The most commonly used line codes add extra transitions in the pattern, to allow proper clock recovery at the receiving end.

Moreover, this type of jitter is accumulative, which means that it increases together with the increase in the number of repeaters looked at.

Jitter due to mapping/demapping

Analog phase variation in tributary signals is sampled and quantized when these are multiplexed in a higher-order signal. This is an inherent mechanism in any TDM system. In SDH, for instance, every 125 μs, certain bytes of the phase are available for adjusting the phase. In short, the phase of tributary signals is quantized.

Also, a tributary signal may be synchronized with a different clock than the clock used to synchronize the aggregate signal that will carry it. The above situations give rise to *phase justification*: Bits of the tributary signal are justified, to align them with the phase of the aggregate signal frame; that is, creating jitter.

Pointer jitter

The use of pointers in SDH/SONET makes it possible to discard the effects of bad synchronization, but these pointer movements provoke an extensive phase fluctuation. Pointer movements are equal to discontinuities in the transported tributaries.

Once the tributary has been extracted, the PLL circuit must continuously adapt itself to bit flows. If the VC-4 pointer has incremented in an STM-1, it will receive 24 bits less, and it must slow down to maintain a constant level for its buffer. If by

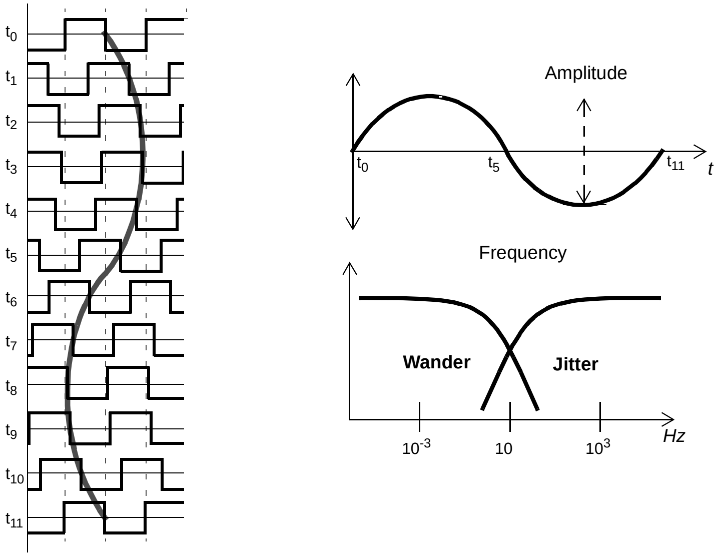


Figure 1.10 A phase fluctuation of a signal is an oscillating movement with an amplitude and a frequency. If this frequency is more than 10 Hz, it is known as jitter, and when it is less than that, it is called wander.

contrast it has decremented, it will receive 24 bits more and should accelerate. As a result, the extracted tributary will contain jitter.

1.3.2.2 Wander

Wander is defined as long-term variations of the significant instants of a digital signal from their reference positions in time (ITU-T Rec. G.810). Strictly speaking, wander is defined as the phase error comprised in the frequency band between 0 and 10 Hz of the spectrum of the phase variation. Wander is difficult to filter when crossing the *phase-locked loops* (PLLs) of the SSUs, since they hardly attenuate phase variations below 0.1 Hz. This is because slow phase variations get compensated with pointer adjustments in SDH/SONET networks, which is one of the main causes of jitter (see Figure 1.10).

Wander brings about problems in a very subtle way in a chained sequence of events. First, it causes pointer adjustments, which are then reflected in other parts of the network in the form of jitter. This in its turn ends up provoking slips in the output buffers of the transported tributary.

The following are the most typical causes of wander:

Changes in temperature

Variations between daytime and nighttime temperature, and seasonal temperature changes have three physical effects on transmission media:

- There are variations in the propagation rate of electrical, electromagnetic or optical signals.
- There is variation of length, when the medium used is a cable (electrical or optical), due to changes between daytime and nighttime or winter and summer.
- There is different clock behavior when temperature changes occur.

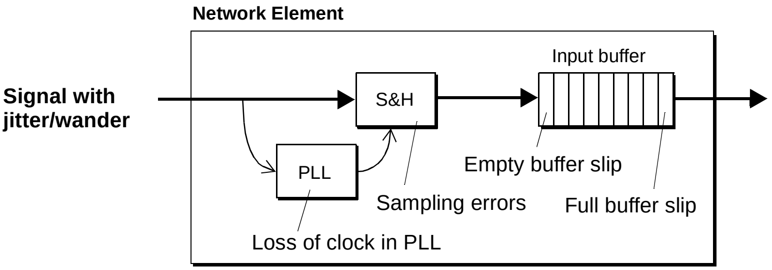


Figure 1.11 Jitter and wander affect every stage of data recovery, producing a number of sampling errors, clock, losses, and overflow.

Clock performance

Clocks are classified according to their average performance in accuracy and offset. The type of resonant oscillator circuit used in the clock source and the design of its general circuitry both add noise, and this results in wander.

1.4 DIGITAL SYNCHRONIZATION AND SWITCHING

Digital switching of *n* x 64-Kbps channels implies that the E1 and T1 frames must be perfectly aligned to make it possible to carry out channel exchange (see Figure 1.12).

The frames are lined by means of a buffer in every input interface of a switch. The bits that arrive at f_i frequency get stored in them, to be read later at the frequency used by the switch, f_o.

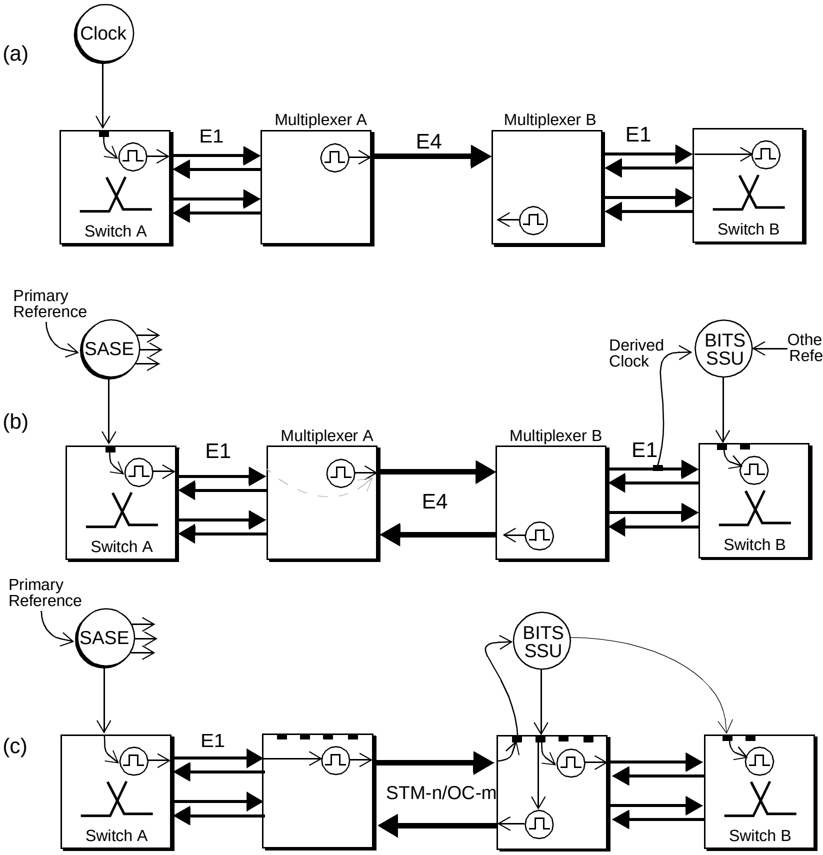


Figure 1.12 Synchronization of two digital centrals: (a) by signal derived from the PDH chain; (b) by PDH and SASE chain; and (c) across SDH network.

But if the clocks are different, $|f_i - f_o| > 0$, the input buffer sooner or later ends up either empty or overloaded. This situation is known as a *slip*: If the buffer becomes empty, some bytes are repeated, whereas if the buffer is overloaded, some valid bits must be discarded in order to continue working. That is to say, slips are errors that occur when PLLs cannot adapt themselves to clock differences or phase variations in frames.

$$f_d = 86{,}000 \times \left| f_i - f_o \right| / n \qquad (slips/day)$$

where
86,400 is number of seconds per day
n: bits repeated or discarded per slip
f_i = *input bit rate*
f_o = *output bit rate*

When effects are caused by slips:

- In the *voice* they are usually not noticed; a click may be noticed when voice is sent compressed;
- In a *facsimile* they may damage many text lines;
- In *modems* they cause microbreaks and may sometimes break the whole connection;
- In *digital TV,* there is loss of color or frame synchronization;
- In *data networks* like SNA, HDLC, frame relay, TCP/IP, there is loss of performance.

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