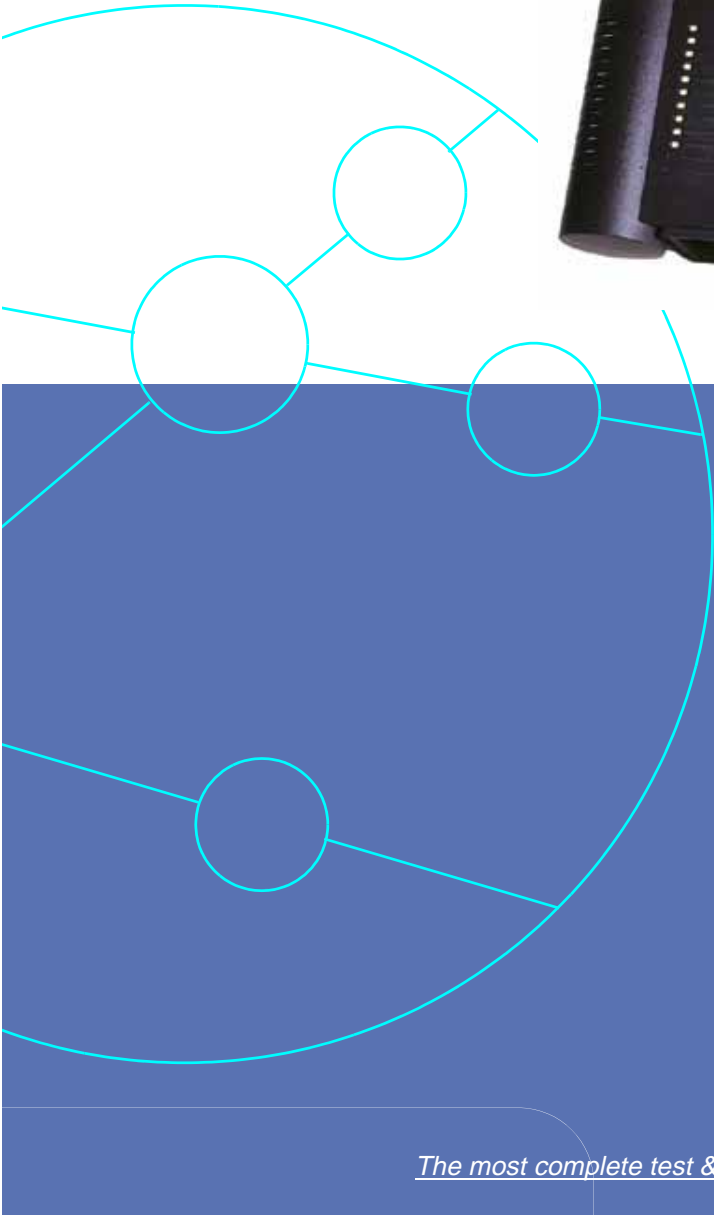


X.50 circuit testing with Victor

X.50 Recommendation defines a framed structure which enables several low rate data channels to be carried within a 64 kbit/s signal. So, X.50 multiplexing scheme allows service providers to transport low rate data of several customers into a single timeslot. Sharing a timeslot between many users rather than use a full 64 kbit/s channel for each one leads to a better and more efficient use of network resources.



Application Note VTX.5020E



The most complete test & measurement portfolio



INTRODUCTION

X.50 Recommendation defines a framed structure which enables several low rate data channels to be carried within a 64 kbit/s signal. So, X.50 multiplexing scheme allows service providers to transport low rate data of several customers into a single timeslot. Sharing a timeslot between many users rather than use a full 64 kbit/s channel for each one leads to a better and more efficient use of network resources.

X.50 defines 3 possible multiplexing structures which have different lengths. The document focuses on structures specified in X.50 division 2 & division 3 which are generated and analysed with Victor.

X.50 OVERVIEW

Since many bits within the multiplexing structure are reserved for framing and status or control purposes the effective bandwidth available for transporting user data is reduced from 64 kbit/s to 48 kbit/s, that is, 25% of multiplex gross bit rate is overhead (16 kbit/s).

X.50 division 2

X.50 division 2 defines a 80-octet frame. Each octet has the first bit

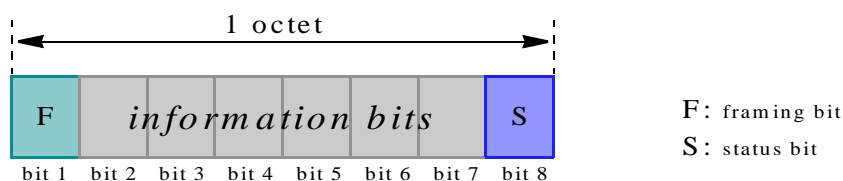
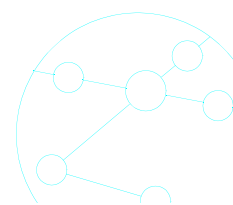


Figure 1

Octet or 8-bit envelope format. Information bits within an octet belongs to a single channel.

reserved for framing purposes, the next 6 bits carry user data and the last bit is a status bit (**figure1**). Data incoming from each individual sub-rate channel is assembled in octets. Therefore, if each sub-rate data channel uses a single octet within the 80-byte frame then 80 different channels at 600 bit/s are carried in a 64 kbit/s mux signal. So each channel will repeat itself every 80th octet

$$64\text{kbit/s} \cdot \frac{1\text{octet}}{80\text{octets}} \cdot \frac{6\text{bits}}{8\text{bits}} = 600\text{bit/s}$$



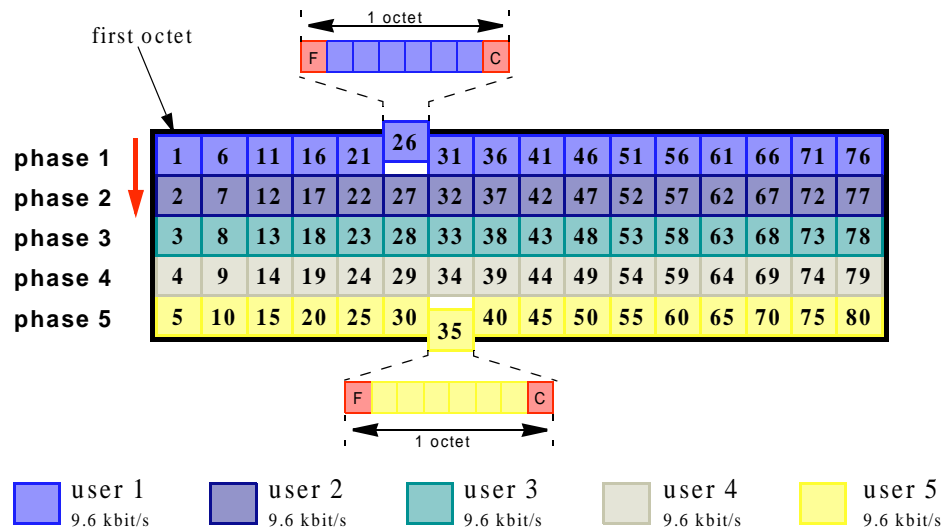


Figure 3 X.50 division 2 frame with a single channel in each phase. Each channel will repeat every octet

Not only channels at 600 bit/s, but also channels at 2.4 kbit/s, 4.8 kbit/s and 9.6 kbit/s are carried within a X.50 division 2 frame. The frame is divided into 5 phases as shown in **figure 2**; each phase will repeat every 5th octet in the transmitted frame. When all octets of a phase are used for a single channel then 5 channels at 9.6 kbit/s are carried in a 64 kbit/s line.

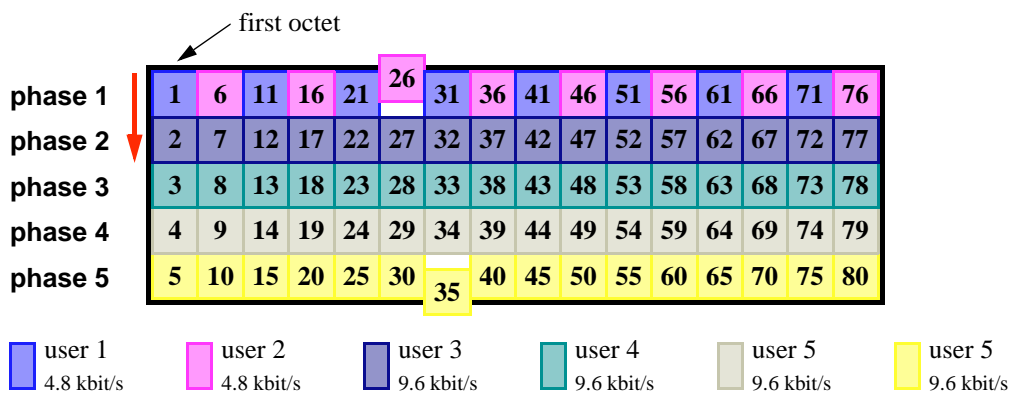
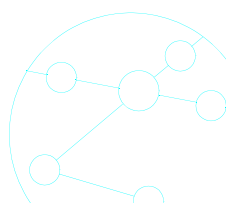


Figure 2 X.50 division 2 frame with phase 1 carrying 2 channels.

However, a phase can be shared by several channels of the same bandwidth. Therefore, the following cases can occur:

- 2 channels at 4.8 kbit/s share a phase. **figure 3**
- 4 channels at 2.4 kbit/s share a phase. **figure 4a**



- 8 channels at 1.2 kbit/s share a phase (not included in X.50 Recommendation). **figure 4b**
- 16 channels at 600 bit/s share a phase.

So, X.50 structures can handle both, homogeneous mixes of subrate channels (with respect to channel rate) and heterogeneous mixtures of subrate channels. Whereas, within a phase only homogeneous mixture of bearer channels is allowed.

Moreover, channels at 19200 bit/s, 28800 bit/s, 38400 bit/s and 48000 bit/s can be achieved by combining several phases together. Although these bit rates are not specified in X.50 Recommendation, they are included in Victor.

As mentioned before, first bit of each octet is reserved for framing information. Therefore, X.50 division 2 frame has 80 framing bits which carry a frame alignment signal and network information. There are 8 bits, "A" to "H", carrying network information. The

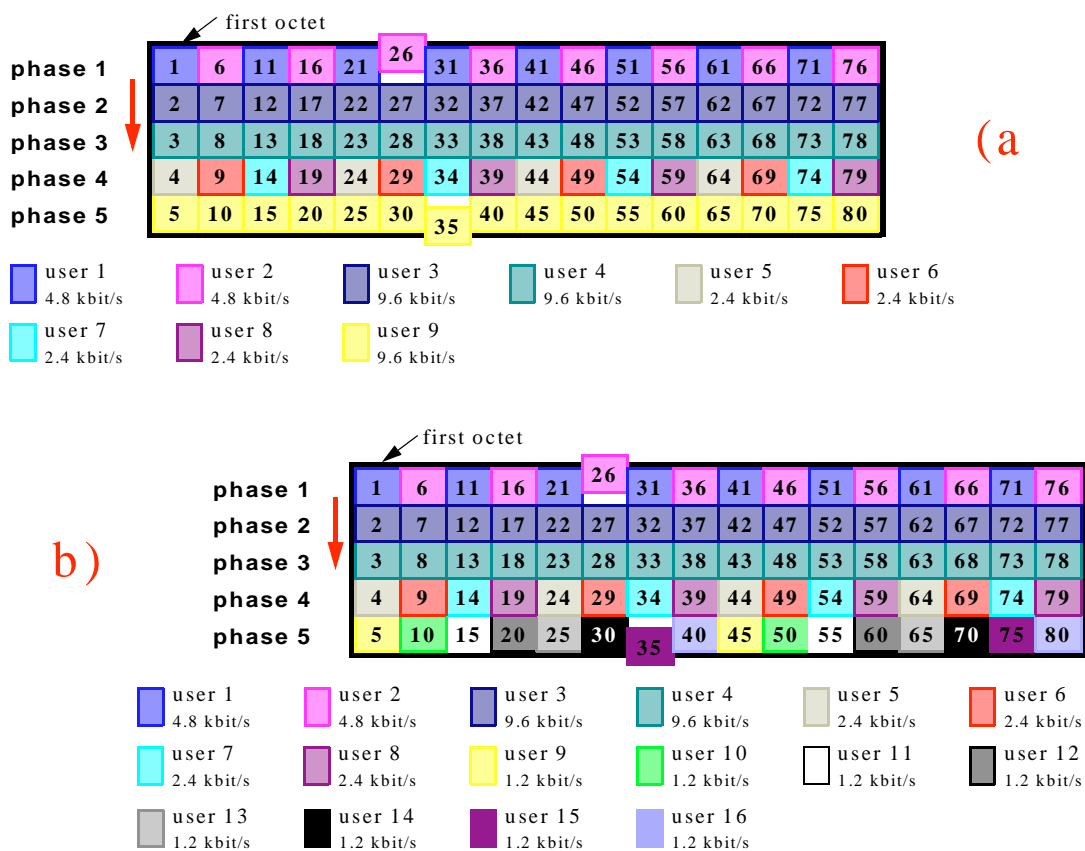
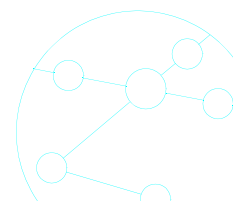


Figure 4

(a) X.50 division 2 frame with heterogeneous mixes of channels at 9.6, 4.8 and 2.4 kbit/s
(b) X.50 division 2 frame with heterogeneous mixes of channels at 9.6, 4.8, 2.4 and 1.2 kbit/s



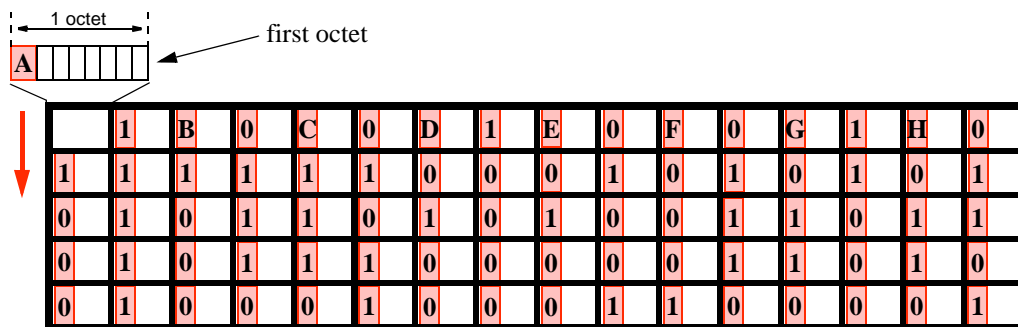


Figure 5

First bit value of each octet. 72 bits carrying framing pattern, A bit used to convey to the end alarm indications and B to H bits reserved to convey further international housekeeping information

remaining bits carry a 72-bit long frame alignment word recommended in CCITT X.50 document. **figure 5**

Currently, only A information bit has a specific function according to CCITT. It is used to indicate alarm condition to the distant end. Alarm condition is declared at the local end when absence of incoming pulses or loss of frame alignment is detected:

- A bit to 1 means no alarm
- A bit to 0 means alarm

X.50 division 3

X.50 division 3 specifies a 20-octet long frame with the same octet format than division 2. If a single octet is used for each channel then 20 channels at 2.4 kbit/s are multiplexed sharing one 64 kbit/s line

$$64\text{kbit/s} \cdot \frac{1\text{octet}}{20\text{octets}} \cdot \frac{6\text{bits}}{8\text{bits}} = 2.4\text{Kbit/s}$$

2,4 kbit/s is the lowest bearer rate of multiplexed channels. However X.50 division 3 frame allows also multiplexing of channels at 9,6 kbit/s and 4,8 kbit/s. Channels at 9,6 kbit/s will repeat every 4th octet. **figure 6**

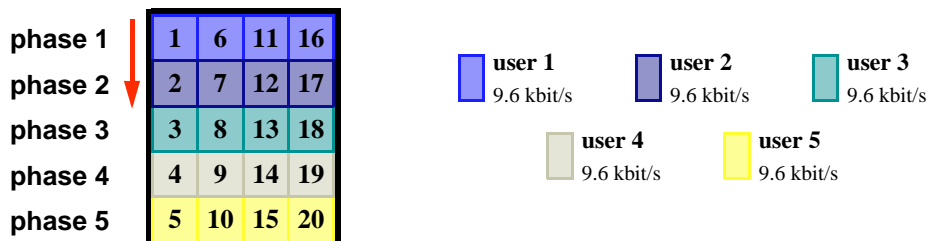
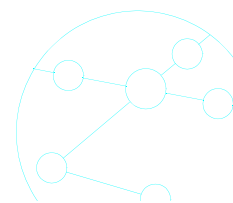


Figure 6

X.50 division 3 frame. A single channel carried in each phase



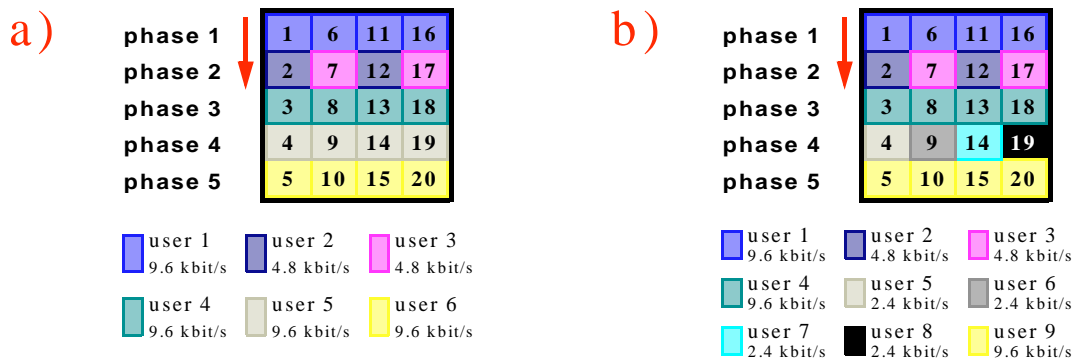


Figure 7

X.50 division 3 frame with (a) 2 channels at 4.8 kbit/s sharing phase 2
(b) 2 channels sharing phase 2 and 4 channels at 2.4 Kbit/s sharing phase 4

Alternatively, within a phase 2 channels can be multiplexed at 4,8 kbit/s or 4 channels at 2,4 kbit/s. **figure 7a & 7b**

The division 3 frame has 20 framing bits. The F bit of the first octet is indicated as “A” and it is also used as alarm information. The remaining bits carry a 19-bit long frame alignment word recommended by CCITT. **figure 8**

Similarly to division 2 structure, multiplexing higher rate channels is achieved by combining phases as a single channel. Thus, channels at 19200 bit/s, 28800 bit/s, 38400 bit/s and 48000 bit/s are carried within a X.50 frame.

X.50 embedded in a 2 Mbit/s signal

The 64 kbit/s X.50 frame can be inserted into the 64 kbit/s rate side of a PCM multiplexer. On the 2 Mbit/s rate side the X.50 frame is carried in one timeslot of the G.704 frame.

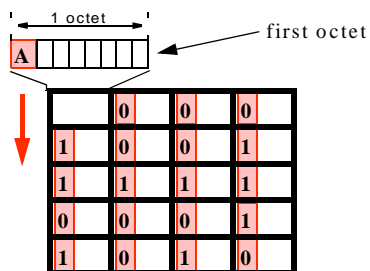
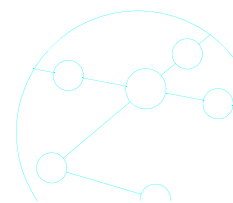


Figure 8

First bit value of each octet in division 3 frame. 19 bits carrying framing pattern and A bit used to convey to the distant end alarm indication



TESTING WITH VICTOR

Victor allows for monitoring and testing X.50 circuits and network elements. Functions are provided for programming and analysing low rate data channels of a X.50 frame which is carried within a timeslot of a 2 Mbit/s G.704 frame. Next applications can be performed.

X.50 Demux testing

Victor enables testing the right end-to-end operation of a circuit with a PCM demux and a X.50 demux.

At the 2 Mbit/s end, Victor's generator side transmits a pattern in a low rate data channel of a X.50 frame which is carried within a timeslot of a 2 Mbit/s G.704 framed signal. The signal is inserted into the higher rate side of the PCM demux. At the other circuit end, on the lower data rate side of X.50 demux, pattern carried in the outgoing data signal is monitored by Victor's analyser side through a data interface such as V.24/V.28 or V.24/V.35. Received pattern analysis provides viewing of circuit operation. **figure 9**

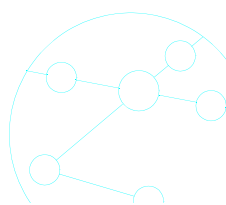
Selection of the multiplexed low rate data channel carrying the test pattern is achieved by choosing manually octets of the X.50 frame, or alternatively, by selecting *phase, rate* and number of channels. Framing bits of X.50 frame A to H as well as the status bits are also programmable.

After the X.50 frame configuration, the G.704 frame timeslot carrying X.50 structure must be also selected. Reach the screen which provides for programming TS contents by pressing firstly the mux block on the setup screen and then the button labelled TS contents.

On the analyser side, just select and program the data interface used for signal reception, and the pattern analyser.

X.50 Mux testing

Alternatively, generating a test pattern through a data interface and inserting it on the low data rate side of X.50 mux then Victor will be able to analyse the test pattern contained in the X.50 frame carried within a timeslot of the outgoing 2 Mbit/s framed signal. Hence, enabling correct end-to-end operation of a circuit with a X.50 mux and a PCM mux to be tested. **figure 10**



Program Victor analyser side to access the channel carrying the test pattern within the X.50 frame. By selecting the *G704&X.50* option in the demux block on the setup screen allows for programming the received frame type division. Selection of X.50 channel carrying pattern is provided by pressing the *pattern* button on the setup screen and choosing *phase*, *rate* and *channel* numbers or alternatively using octet by octet selection.

Monitoring & testing X.50 circuits

Simultaneous generation and analysis of 2 Mbit/s framed signals carrying a X.50 frame allows for out-of-service testing of low rate data channels in 2 Mbit/s circuits with digital cross-connects (DXC).

In-service measurements in 2 Mbit/s circuits carrying a X.50 frame are also possible. Loss of X.50 frame synchronization, framing pattern error detection and remote alarm condition (A bit) are indicated via SoftLEDs and/or audible alarm. Besides counters, rates and histograms are also provided. On the measurement screen, press the X.50 button and values of A to H bits and the status bits for each channel are displayed.

Victor enables BER, BLER tests and performance analysis according to G.821 to be carried out. In out -of-service condition, measurements are performed based on the transmitted test pattern.

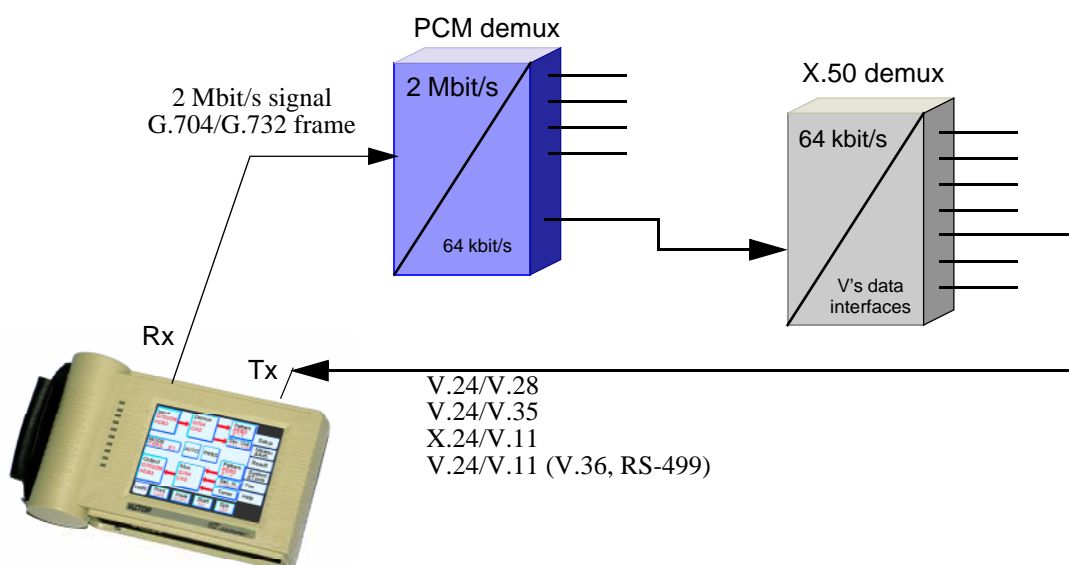


Figure 9

End-to-end circuit with PCM and X.50 demux testing

