



Combined jitter test for SDH/SONET

The two main causes of jitter are mapping jitter and pointer jitter, which together are known as combined jitter. Mapping jitter is inherent to SDH/SONET networks while pointer jitter is caused by pointer adjustments.



Application Note ANVAJWG7831e



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The two main causes of jitter in SDH/SONET networks are the result of two processes:

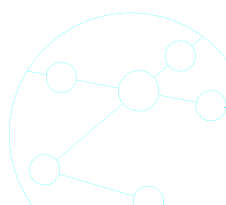
- a) *mapping jitter* caused by loading tributaries in the synchronous structures (containers or synchronous payload envelopes)
- b) *pointer jitter* caused by pointer adjustments suffered in the generation of SDH and SONET frames.

To a greater or lesser degree, *mapping jitter* is always present in synchronous signals, and when pointer movements occur this creates *pointer jitter*. Together, both of these effects, pointer and mapping jitter, are known as *combined jitter*.

MEASURING MAPPING JITTER

The aim of the measurement is to quantify the jitter produced when PDH/T-Carrier payload is added to an SDH/SONET data stream. The bit rate of the signals to be multiplexed admits a tolerance range. As the clock frequency takes values inside the range there is a frequency offset regarding to the nominal bit rate. This forces an adaptation process in the multiplexer. Due to the stuffing bits necessary to adapt the plesiochronous signals to the containers or SPE payloads, a jitter is present in the receiver clock. This jitter cannot be deleted completely by the recovery timing circuit (PLL), and remains in the plesiochronous tributary demultiplexed.

The figure above is a measurement setup for mapping jitter. A frequency offset at the limits of the range has been included in the signal generated to stress the device under test and to force the maximum amount of mapping jitter when in-range operation. The same tributary is recovered by the analyzing section to measure jitter in the corresponding band. (this is fixed by the recommendations for every bit rate, e.g. for 2 Mbit/s ITU G.823 defines the maximum jitter allowance as 0.075 UIpp in the measurement band from 18 kHz to 100 kHz). The test set and the device under test have been synchronized to



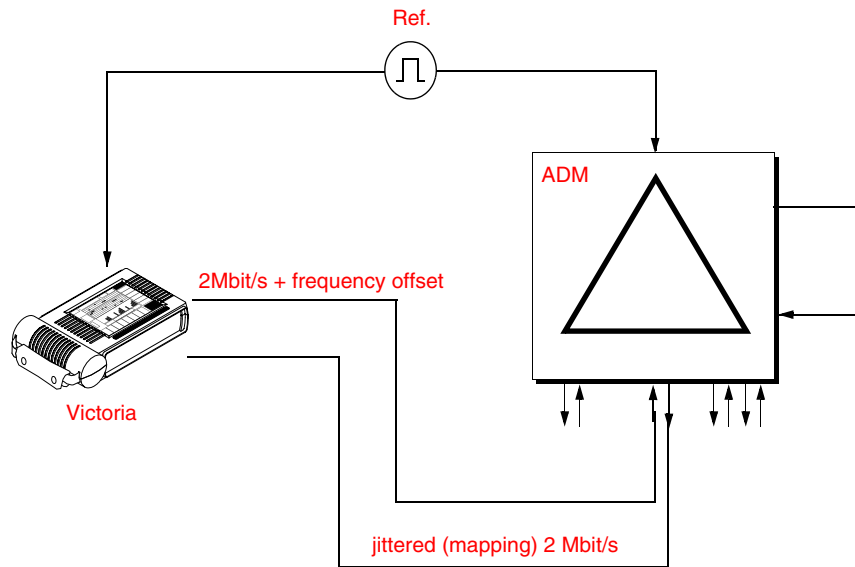


Figure 1

Mapping jitter test setup

a common reference to avoid uncontrolled jitter adjustments which would add pointer jitter to the measurement.

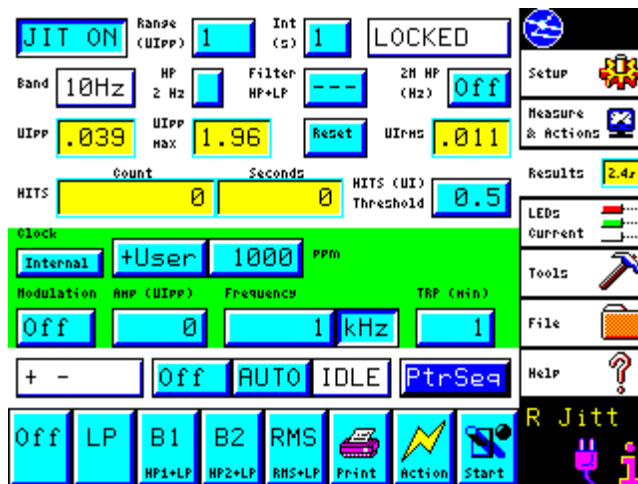
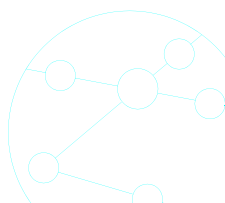


Figure 2

Jitter measurement results screen in Victoria: selecting the jitter measurement filter

Mapping jitter is always present in jitter measurements in which plesiochronous signals are embedded in synchronous signals, however, pointer mechanism in SDH/SONET introduces pointer jitter, with is



an order of magnitude higher than mapping jitter, and the main jitter component of *combined jitter*

GENERATING POINTER SEQUENCES

To test combined jitter in a network elements like an SDH/SONET multiplexer we need to generate a sequence of pointer movements to stress and then drop a tributary, in order to analyze the resulting combined jitter (remember that mapping jitter is always present).

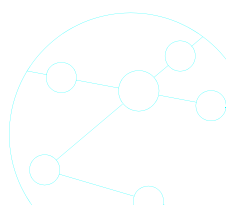
The frequency offset, diurnal wander, clock noise and originator jitter cause pointer adjustments. The phase variation signal will be the sum of the several causes. Analytical prediction of accumulated pointer activity is very difficult. To achieve some level of confidence in accumulation properties and the consequences standard bodies have developed extensive simulations: ITU-T G.783 and ANSI T1.105.03 define a set of pointer sequences.

G.783 Identifier	Pointer adjustments	Mnemonic
a	Single of opposite polarity	+-
b	Regular plus one double	+"&Add
c	Regular with one missing	+"&Cancel
d	Double of opposite polarity	+++
e	Single	+
f	Burst	+++Burst
g/part 2	AU periodic 87-3 pattern	+87/3
g/part 3	AU periodic 87-3 Add position	+87/3 & Add
g/part 4	AU periodic 87-3 Cancel position	+87/3 & Cancel
h/part 1	Periodic	+Periodical
h/part2 Add	Periodic Add position	+Periodical & Add
h/part 2 Cancel	Periodic Cancel position	+Periodical & Cancel

Figure 3

Pointer sequences as defined by ITU-T G.783. The third column is the mnemonic used in Victoris

These models take into account the combination of sources of phase variation to stress the pointer processing circuits in the network elements, and to perform predefined jitter measurements. G.783 sequences, as well as the inverted variants included by Victoria and the



corresponding mnemonics are listed in the corresponding screen of the Victoria graphical user interface, as shown in the figure below.

The pointer sequences are regular streams of pointer adjustments (increments, decrements) modified by some different operations (e.g. pointer increments - consecutive increments separated by smaller intervals-). Basically, there are two types of sequences defined in the above mentioned recommendations.:

- single/burst pointer adjustment sequences: To simulate reconfigurations in the synchronization of the network (e.g. when a network element switches from a synchronization source to another forces one or more pointer movements)
- regular/periodic pointer adjustment sequences: To simulate the behavior of the network elements when synchronization is lost and enter in holdover mode, producing continuous pointer adjustments. In addition to this fact, pointer movements can be produced due to phase noise from the other nodes of the network so, to the continuous pointer movements, an added or canceled adjust is performed regularly.

Real measurements have demonstrated that, when losing synchronization, gaps are introduced in the pointer sequence generated. It is the case of VC-4 cross-connection, in which a repetitive sequence of 87 evenly spaced pointer adjustments is followed by 3 missing pointer movements. This is the reason for the 87/3 sequences (G.783 ITU-T recommendation).

The structure of the sequences, as described in G.783 is defined by three intervals:

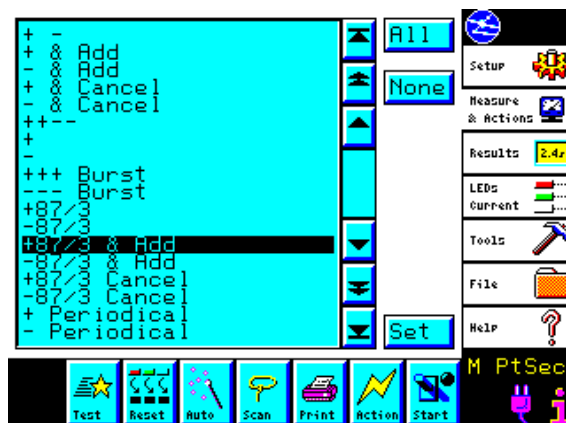
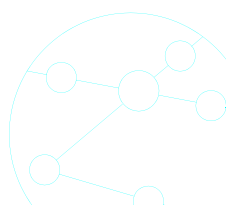


Figure 4

Pointer sequences predefined in Victoria.



1. Initialization interval: To force the pointer processor, buffers in the network element are filled so that the effects of the test sequence can be measured. This ensures the repeatability of the measurements.
2. Cool-down interval: Ensures that the equipment clock recovery circuit and the desynchronizer have become adapted to a steady state of regular pointer sequence or absence of pointer movements. Thus, the equipment is adapted to the pointer sequence.
3. Measurement interval: The timed period over which the measurement of sequence effects is performed.

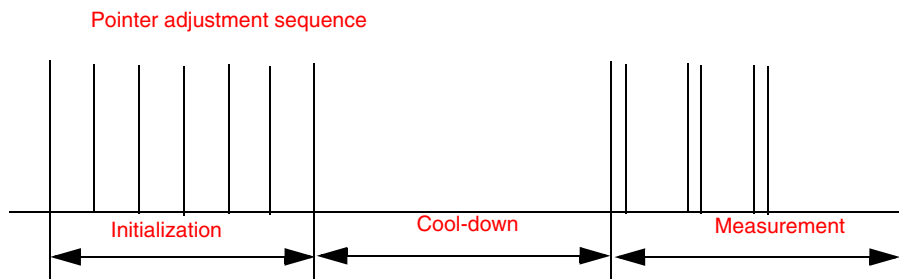


Figure 5

Example of pointer adjustment sequence: the vertical bars symbolize an increase in the pointer value. The x-axis is the time.

Just push the button *Printer Sequence* after the sequence selection and select the sequence desired (see figure 4) to stress the network element.

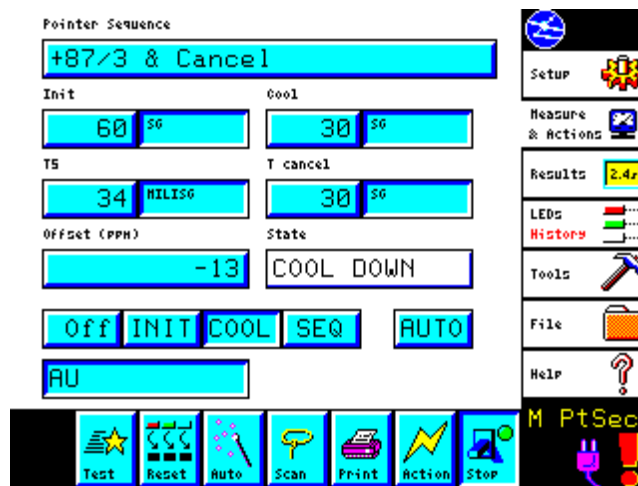
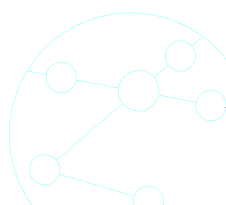


Figure 6

Periods of initialization (to assure the buffer of the NE pointer processor is filled,) and cool-down (a period for the clock recovery circuit and desynchronizer) can be programmed as defined by the recommendation ITU-T G.783). Intervals between pointer movements can be programmed too. Additionally there exists the possibility of introducing an offset on the tributary to be mapped.

The screen in the figure above includes the possibility to introduce a frequency offset in the test tributary. This adds mapping jitter to the generated signal and permits a second variant of the mapping jitter test setup, following the same setup of the figure 7 but with the aggregate



signal generated (STM-N or STS-M) including a frequency offset in the tributary tested (e.g. E1 or T1) and without using the pointer sequences.

MEASURING COMBINED JITTER

As mentioned above, to measure the efficiency of a NE to compensate the effects of pointer jitter, special pointer adjustment sequences defined by G.783 are used. As pointer jitter cannot be measured separately from mapping jitter, the jitter actually measured is the combined jitter. Combined jitter appears in the tributary signals once they are dropped from their synchronous aggregate signals. The measurement diagram is shown in the figure below. As in the mapping jitter setup, both the test set and the device under test (ADM in the example) are synchronized to a common source to avoid any uncontrolled pointer adjustments (all the ones generated come from G.783 sequences).

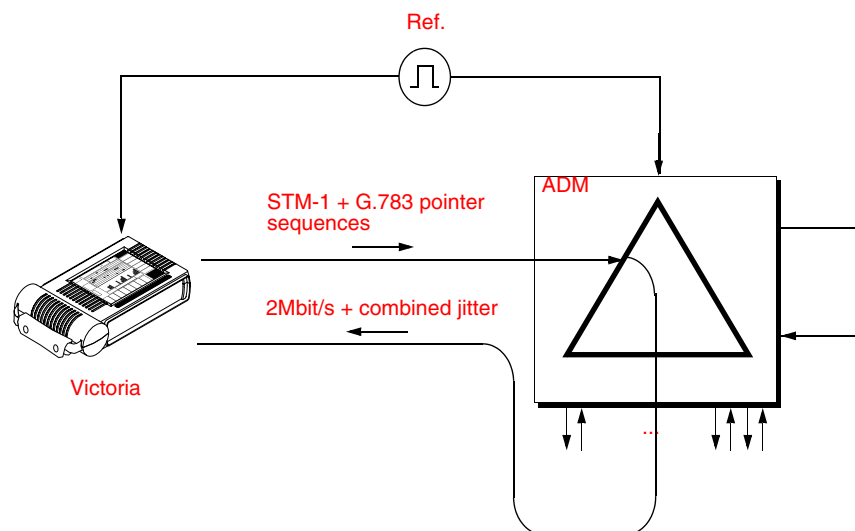
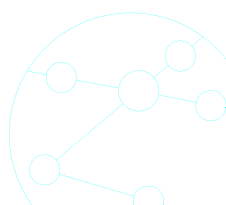


Figure 7

Pointer (combined) jitter test diagram: example with an SDH ADM.

The features of Victoria Jitter/Wander include the capability of performing combined jitter measurements both generating the necessary pointer sequences and analyzing the jitter at the tributary outputs.

Victoria is compliant with ITU-T O.172 and O.171 recommendations, which define the test instrument for jitter/wander measurements in synchronous and plesiochronous networks, including all the capabil-



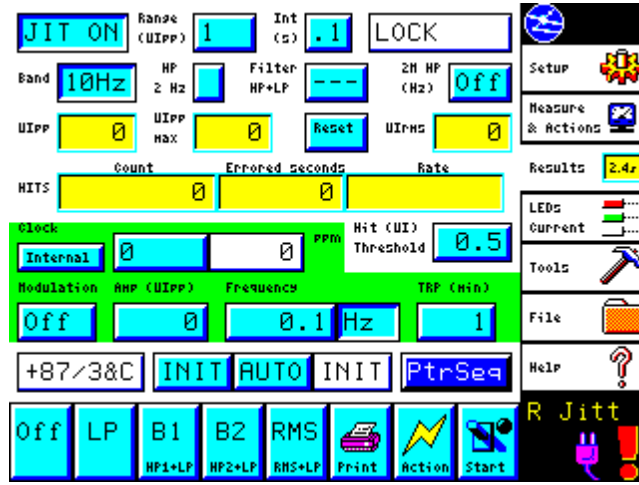


Figure 8

Jitter results screen: instantaneous Uipp value, max Uipp value, RMS amplitude and hits are displayed. Jitter amplitudes (Uipp and UIrms) vs. time are traced by the instrument too.

ities needed for currently demanded measurements in the field of jitter and wander. □



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